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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jeffrey S. Mailloux et al.

Title: MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE SELECTION CIRCUITRY

Docket No.: 303.623US3
Filed: December 3, 1997
Examiner: Hong C. Kim

Serial No.: 08/984,562
Due Date: February 4, 2003
Group Art Unit: 2186

Box AF
Commissioner for Patents
Washington, D.C. 20231

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APPELLANTS' BRIEF ON APPEAL

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In re Application of:		
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APPELLANTS' BRIEF ON APPEAL

Box AF
Commissioner for Patents
Washington, D.C. 20231

Sir:

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on December 4, 2002, from the Final Rejection of claims 22-32, 59, 61, 63, and 66-72 of the above-identified application, as set forth in the Final Office Action mailed October 23, 2002.

This Appeal Brief is filed in triplicate. The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $320.00 which represents the requisite fee set forth in 37 C.F.R. § 117(c). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims 22-32, 59, 61, 63, and 66-72.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the Assignee, Micron Technology, Inc.

2. RELATED APPEALS AND INTERFERENCES

There are no interferences known to Appellants, Appellants' legal representative, or the Assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter.

There is one appeal known to Appellants, Appellants' legal representative, or the assignee that may directly affect or be directly affected by or have a bearing on the Board's decision in the appeal in this matter. This related appeal is currently pending before the Board and concerns U.S. Patent Application Serial Number 08/984,561.

3. STATUS OF THE CLAIMS

Claims 22-32, 59, 61, and 63-72 are currently pending. Claims 22-32, 59, 61, 63, and 66-72 stand rejected and are appealed. Claim 65 stands allowed. Claim 64 is objected to as being based on a rejected claim, but is deemed allowable if rewritten in an independent form.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action mailed October 23, 2002.

5. SUMMARY OF THE INVENTION

As described in the Appellants' specification at page 7, line 6 - page 8, line 13, and shown generally in figures 9-11, embodiments of the invention disclosed relate to a memory device that selectably operates in either burst or pipelined modes. In one embodiment, an asynchronously addressable storage device 100 (Application, FIG. 9) includes mode circuitry 121 configured to select between burst and pipelined modes, and circuitry 122 operable in either the burst mode or pipelined mode and configured to switch between the burst mode and the pipelined mode for operating the device 100 in either mode. (Application, Pg. 29, lines 5-25).

Some embodiments of the invention can switch between burst access and pipelined modes of operation without ceasing ("on the fly"). (Application, Pg. 33, lines 17-19). In the burst mode of operation, an externally-generated memory address stored in the circuitry 122 is used to select data within the device 100. A counter 149 included in the circuitry 122 increments the stored external address to internally generate addresses for subsequent accesses. In the pipelined mode of operation, the circuitry 122 uses only external addresses 115 to access data within the device 100. (Application, Pg. 29, lines 8-16). As address information passes through the memory, it is operative in one operational area before moving into another operational area. However, once moved, another set of address information may enter the operational area exited, and accesses to memory may overlap without conflicting. (Application, Pg. 8, lines 1-5). In addition to the embodiment described, other embodiments of varying scope, including systems, methods, and storage devices, such as memory circuits, are discussed. (Application, Pg. 33, line 23 - Pg. 40, line 19).

6. ISSUES PRESENTED FOR REVIEW

1) Whether claims 22-32, 59, 61, and 66-72 were properly rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 5,610,864, issued to Manning (hereinafter Manning (864)).

2) Whether claims 22-32, 59, 61, 63, and 66-72 were properly rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,729,503, issued to Manning (hereinafter Manning (503)) in view of Manning (864).

7. GROUPING OF CLAIMS

All claims are to be taken independent of each other and each stands alone for purposes of this appeal.

8. ARGUMENT

a) The Applicable Law

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> To establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

While it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d (BNA) 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. (BNA) 171, 174 (C.C.P.A. 1979)). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). Thus, the references must be considered in their entirety, including parts that teach away from the claims. See § MPEP 2141.02.

b) The References

Manning (864): teaches a memory device which can be accessed using latched row and column addresses. (Col. 4, lines 10-28). The device may also be accessed using a high-speed burst mode of operation, wherein the address is incremented internal to the device, using transitions of the column address select (/CAS) signal, following the assertion of a single external column address. (Col. 4, lines 29-49). Switching between the burst extended data out (EDO) mode and the standard EDO mode is described. (Col. 6, lines 14-22). Switching between interleaved and linear addressing modes is mentioned. (Col. 6, lines 30-34). The possibility of applying a pipelined architecture is also mentioned. (Col. 5, lines 43-46). Operation of the pipelined architecture is said to be characterized by having a memory throughput of less than one access per cycle, such that the data coming out of the device is offset by some number of cycles equal to the pipeline length. (Col. 5, lines 46-50). However, no details of the structure of the architecture, how it is applied, or its operation, are given.

Manning (503): describes a synchronous memory device having burst mode access and page mode access capabilties. (Col. 3, lines 3-4). In more complex versions of the device, fast page mode, EDO page mode, and static column mode may also be selected. (Col. 6, lines 52-56).

c) Discussion of the Rejections

***c.1* -- The rejection under § 102**

Claims 22-32, 59, 61, and 66-72 were rejected under 35 USC § 102(e) as being anticipated by Manning (864). First, the Appellants do not admit that Manning (864) is prior art and reserve the right to swear behind this reference in the future. Second, the Appellants respectfully submit that a case of anticipation under 35 U.S.C. § 102(e) has not been made because Manning (864) does not disclose each and every element of claims 22-32, 59, 61, and 66-72. Therefore, the Appellants respectfully traverse this rejection under 35 U.S.C. § 102(e).

c.1.1. Why the reference does not disclose each and every element of the claimed subject matter as arranged in the claims.

Manning (864) specifically does not disclose "control logic for providing a ... mode control signal" and "a multiplexer ... for receiving ... the ... mode control signal ... therefrom and for switching the memory circuit between a burst mode and a pipelined mode", which is explicitly claimed by the Appellants in claims 22-32, and 59; or "control logic for providing [a] ... mode control signal" that is ultimately used to switch between, or indicate, burst and pipelined modes of operation, as claimed by the Appellants in claims 66-72. Further, with respect to claim 61, Manning does not disclose control logic for providing an *internal* mode control signal (Manning only speaks to the use of *external* mode control signals).

Several assertions were made in the Office Action mailed to the Appellants on October 23, 2002 which attribute support to various concepts allegedly disclosed by Manning (864). However, a careful reading of each citation reveals that the description of the asserted elements in the Office Action is incorrect. These assertions have been made with respect to:

Claims 22, 59, and 66 - Manning (864) does not disclose providing or receiving a mode control signal, or circuitry for switching or selecting between a burst mode and a pipelined mode (Manning (864) never discusses switching or selecting between the modes, only operation in

burst and standard EDO modes, and the possibility of using a pipelined architecture). While references to Manning (864) col. 6, lines 26-34 are made to support operation in the pipelined mode, this portion of the reference is actually directed solely to EDO operations. In fact, the Office has specifically admitted this defect in Manning (864) in other Office Actions, such as the Office Action mailed to the Appellants on July 18, 2001 (Paper 19, page 7) for application serial no. 08/984,701, wherein the statement is made that "*Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation.*"

Claim 23 - Manning (864) does not disclose an external mode select signal for selecting the burst mode or the pipelined mode (the cited portion merely discusses switching between burst and standard EDO modes, or between interleaved and linear addressing modes; and FIG. 1 element 38 represents an *internal* signal, not an external signal).

Claims 25 and 70 - Manning (864) does not disclose using write enable and a separate *output enable* signal for determining the mode control signal (Manning only discusses using the write enable (/WE) and row address select (/RAS) signals for this purpose).

Claim 28 - Manning (864) does not disclose using a second external address subsequent to a first external address for operating in the pipelined mode (Manning never discloses how a pipelined *architecture* might operate).

Claims 29 and 72 - Manning (864) does not disclose a pipelined mode, nor is the pipelined mode disclosed as being an EDO mode, as claimed by the Appellants (Manning never discloses how a pipelined *architecture* might operate).

Claims 30-31 - Manning (864) does not disclose any type of address strobe latency in conjunction with pipelined mode operations (Manning never discloses how a pipelined *architecture* might operate).

Claims 61- Manning (864) does not disclose a multiplexer coupled to ... control logic for reeiving ... the internal mode control signal" as claimed by the Appellants (Manning only speaks to the use of *external* mode control signals).

c.1.2. Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning (864) does not disclose these elements, how (specifically) does Manning (864) support *switching* or *selecting* between, or indicating burst and pipelined modes of operation, as claimed in claims 22, 59, and 66 (and in all claims that depend from them)?

Second, a case of anticipation has not been established. While the assertion is made that Manning (864) discloses circuitry for "switching the memory circuit between a burst mode and a pipelined mode", and "a multiplexer", the Appellants' representative, after a careful study of Manning (864), was unable to locate any such discussion, nor any such circuitry which was configurable to select or switch between burst and pipelined modes of operation.

For example, the only citations offered by the Office to support the assertion that Manning (864) discloses "switching between a burst mode and a pipelined mode" with respect to claims 22, 59, and 66 are: col. 5, lines 41-50; col. 6, lines 14-34; and col 7, lines 43-54. Col. 5, lines 41-50 discusses the possibility of using a pipelined architecture, but not as enabling switching between pipeline or burst operations within the *same* memory, as disclosed and claimed by the Appellants. Col. 6, lines 14-34 merely describe burst and standard EDO operations (i.e., page mode - see col. 6, lines 18-19). Finally, col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning (864) never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, or circuitry to effect such a selection, as claimed by the Appellants in independent claims 22, 59, and 66, and all of the claims which depend from them. As noted above, *this fact has been admitted by the Office.*

In short, what is discussed by Manning (864) is not identical to the subject matter of the embodiments claimed, as required by the M.P.E.P., and therefore, the rejection under § 102 is

improper. Reconsideration and allowance of claims 22-32, 59, 61, and 66-72 is respectfully requested.

***c.2* -- The rejection under § 103**

Claims 22-32, 59-61, 63, and 66-72 were rejected under 35 USC § 103(a) as being unpatentable over Manning (503) in view of Manning (864). First, the Appellants do not admit that Manning (864) or Manning (503) are prior art and reserve the right to swear behind these references in the future. Second, because the devices and methods taught in the references are not the same as that claimed by the Appellants, and can not be combined to operate as such, since there is no evidence in the record to support combining the references, and finally, since Manning (864) and Manning (503) teach away from any such combination, the Appellants respectfully traverse this rejection under § 103 by the Office.

Manning (503) does not disclose selecting or switching between burst and pipelined modes. As noted above, Manning (864) also does not disclose switching between burst and pipelined modes, as claimed by the Appellants. While the possibility of using a pipelined architecture in his invention is described, no details as to how this might be accomplished, or how such a device might operate, are given. Manning (864), Col. 5, lines 43-50.

The Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning (864) does not disclose these elements, how (specifically) does Manning (864) support *switching* or *selecting* between burst and pipelined modes of operation? Manning (864) Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning (864) Col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, Manning (864) never discusses the ability to *select* or *switch* between burst and pipelined modes of operation, as claimed by the Appellants.

Another way of viewing this issue is to ask the question: How can a memory have a pipelined architecture (as mentioned by Manning (864)) without inherently operating in the pipelined mode (as claimed by the Appellants)? The brief answer is that a memory, such as a

burst EDO memory, may include pipelined registers that permit the rapid generation of *internal* addresses. However, *external* addresses are still received and processed in the same fashion as regular EDO memory. See, for example, the definition for "Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999, attached hereto as part of Appendix II.

In memory terminology, a row of memory cells is called a page. With page-mode memory, a row address is applied to the chip and the RAS signal held active while sequential column addresses are applied and the CAS signal cycled until an entire row of memory cells are read or written. By addressing columns in this manner, all of the memory cells in a selected row can be written or read without changing the row address. Since page-mode memory requires a setup time for each column address, it was eventually replaced with fast page-mode memory.

Fast page-mode memory eliminates most of the setup time for column addresses within a page, so it is faster and consumes less power than page-mode memory. With fast page-mode memory, memory accesses for an entire page were usually fast enough to reduce wait states in processors available for use with this type of memory. However, when the processor requests data from a different page, both row and column addresses have to be changed, and the resulting delay is similar to ordinary page-mode operation. See "Fast Page Mode (FPM)", Id.

EDO memory is similar to fast page-mode memory in that an entire page of memory can be read very quickly. The major advantage of EDO memory is that it modifies CAS timing to hold data at the chip's output pins longer. This means that the output data can be read while the CAS signal is de-asserted and set up for the next cycle, resulting in less waiting. With EDO memory, data can be read or written (within a page) as fast as the memory chip will accept new column addresses. EDO allows more overlap between column accesses and data transfers than fast page-mode memory, eliminating most of the wait and resulting in a considerable performance improvement. See "Extended Data Output RAM (EDO)", Id.

Burst EDO memory further improved EDO performance by adding **a pipeline stage** (i.e. **a pipelined architecture**) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more sequential addresses (within a page). This address circuitry eliminates the time required to detect

and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture does not accept external addresses so as to operate in a pipelined mode (as defined by the Appellants in the Application). See "Burst Extended Data Output RAM (BEDO)", Id.

In embodiments of the Appellants' invention, a newburst signal from control logic is described. The newburst signal is fed to a multiplexer for choosing which type of addressing is to occur. For one type of addressing, burst operation is provided beginning with an initial external address stored in a temporal storage device. Consequently, if burst operation is the selected mode of operation, then a counter is used to increment the initial external address. (Application, Pg. 29, lines 8-25)

In pipelined mode, address information is divided into operational times. As address information passes through a memory, it is operative in one operational area before moving onto another operational area. However, once moved, another set of address information may enter the operational area exited. Thus, by time slicing address information, accesses to a memory may overlap without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Therefore, **internal addresses are not generated in pipelined mode**. Rather, addresses are provided from an external source as a stream of data. In page mode, with one enable signal held active and another enable signal cycled, an external address is received on each cycle of the cycled enable signal. For example, if /RAS is held active, and /CAS is cycled, a random or determined order of columns associated with the row address may be accessed in pipelined mode, whereas in burst mode, a predetermined pattern of columns may be accessed. (Application, Pg. 8, lines 1-13)

Manning (503) teaches synchronous (not asynchronous) standard EDO, fast page mode EDO, and burst EDO modes of operation. As admitted by the Office, Manning (503) "does not specifically disclose a pipeline mode." Paper 29, pg. 7, lines 1-2. Thus, it would be impossible for Manning (503) to suggest or teach switching between a burst and a pipelined mode of operation. The Appellants can find nothing in the specification of Manning (503) to support asynchronously switching between burst and pipelined modes of operation. Instead, the device operates as a synchronous burst access memory device, as is clear from a reading of the Manning (503) title and disclosure. Since no mention is made in any of the references to asynchronously

switching, selecting, or choosing between burst and pipelined modes of operation, combining Manning (864) and Manning (503) does not result in a device having asynchronously selectable burst and pipelined modes of operation. It is only hindsight gained from the Appellants' disclosure which enables providing both burst and pipelined modes of operation in a single asynchronous memory device, and switching therebetween at will.

Considering that Manning (503) does not teach switching between a pipelined mode and a burst mode, and the lack of description given by Manning (864) with respect to implementation of a pipelined architecture, it is respectfully submitted that a *prima facie* case of obviousness has not been established with respect to independent claims 22, 59, 63, and 66. This is because the combination of Manning (864) and Manning (503) does not teach each and every element of claims 22, 59, 63, and 66, as well as the claims that depend from them. Therefore, claims 22, 59, 63, and 66 should be allowable over any combination of Manning (503) and Manning (864). It is also respectfully noted that since claims 23-32, 64, and 67-72 depend from respective claims 22, 59, 63, and 66, these dependent claims are allowable for at least the same reasons, since any claim depending from a nonobvious independent claim under 35 U.S.C.§ 103 is also nonobvious. See M.P.E.P. § 2143.03.

Turning now to the other independent claim, claim 61, it can be seen that neither Manning (864) nor Manning (503) teaches "a multiplexer coupled to ... the control logic for receiving the ... internal mode control signal ... for switching the memory circuit between a first mode of operation and a second mode of operation." Thus, it is respectfully submitted that this independent claim is also allowable over the combination of Manning (864) and Manning (503).

Further, it is improper to combine Manning (864) and Manning (503). Manning (503) teaches a synchronous memory device. *See*, for example, the Title of Manning (503). Manning (864) is directed toward an asynchronous memory device. The M.P.E.P. requires that the asserted combination of the references must not render the prior art unsatisfactory for its intended purpose, or change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. One of ordinary skill in the art would not be led to combine the dissimilar operation of these two references because doing so would clearly change the fundamental principle of operation for each device disclosed, rendering one or the other unfit for its intended purpose. In

addition, it is improper to combine references where the references teach away from their combination. See M.P.E.P. § 2145(X)(D)(2). In this case, each reference teaches away from the other: Manning (864) teaches asynchronous operation, while Manning (503) teaches synchronous operation.

Still further, the only reason given to combine the references so as to provide an asynchronous memory device which supports switching between a burst and pipelined mode of operation is because one of ordinary skill in the art would be "lead to an obvious fashion to provide a pipelined page mode circuitry since Manning, '864 discloses that the current invention include a pipelined architecture (col. 5, lines 43-49) which would increase processing speed." This assertion completely ignores the fact that Manning (864) and Manning (503) are directed to two different types of memory. Since no reference is supplied to support this assertion, as required by the *In Re Sang Su Lee* court, it appears the Examiner is using personal knowledge, and the Examiner is thus respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Finally, as was disclosed in the Application and noted in a several previous responses to various Office Actions in this matter, it is a specific unaddressed problem of asynchronous DRAMs to switch between burst and pipelined modes of operation, since it was not previously needed (see Application, page 5, lines 16-22). Manning (503), describing a synchronous memory, most certainly is not directed toward the solution of this problem.

Since combining the references is improper, since any combination of the disclosed concepts would be inoperative, since the cited references fail to teach all aspects of the Appellants' invention as claimed, and since the references teach away from the combination asserted by the Office, a case of obviousness has not been established, and the Appellants respectfully request reconsideration and withdrawal of the rejection of claims 22-32, 59, 61, 63, and 66-72 under 35 U.S.C. §103.

c.3 Why the claims are separately patentable:

While the separate patentability of each claim has been discussed in the "argument" section above, as allowed in the M.P.E.P. § 1206, the reasons are summarized here to ensure completeness and as a matter of convenience for the Board.

Independent claim 22 includes a memory circuit having "control logic for providing a selected mode control signal" and "a multiplexer coupled to the ... control logic for receiving the ... mode control signal ... and for switching the memory circuit between a burst mode and a pipelined mode". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements.

To the elements of independent claim 22, dependent claim 23 adds "logic ... to receive an external mode select signal for selecting the burst mode or the pipelined mode". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 22, dependent claim 24 adds "mode circuitry for providing the ... mode control signal ... coupled for receiving an enable signal for determining the ... mode control signal." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To this dependent claim 24, dependent claim 25 further adds an "enable signal selected from ... write enable and output enable signals." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 22, dependent claim 26 adds "selection and temporary storage circuitry ... coupled to a counter ... for switching the memory circuit between a burst mode and a pipelined mode." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To dependent claim 26, dependent claim 27 further adds a counter "used for incrementing the first external address when in the burst mode." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To dependent claim 26, dependent claim 28 further adds selection and temporary storage circuitry coupled for receiving subsequent external addresses "for operating in the pipelined mode." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of

elements.

To dependent claim 28, dependent claim 29 further adds "the pipelined mode and the burst mode are extended data out modes." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To dependent claim 29, dependent claim 30 further adds that "the pipelined mode and the burst mode have no column address strobe cycle latency during a write cycle." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To dependent claim 30, dependent claim 31 further adds that "the pipelined mode and the burst mode have at least a two column address strobe cycle latency during a read cycle." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

To dependent claim 26, dependent claim 32 further adds incorporation of the memory circuit in an asynchronously-accessible random access memory. Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

Independent claim 59 includes an "asynchronous dynamic random access memory circuit" having "control logic for providing a selected mode control signal" and "a multiplexer coupled to the ... control logic for receiving the ... mode control signal ... and for switching the memory circuit between a burst mode and a pipelined mode". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements.

Independent claim 61 includes a memory circuit having "control logic for providing an internal mode control signal" and "a multiplexer coupled to ... selection and temporary storage circuitry and to ... control logic for receiving the first external address and the internal mode control signal respectively therefrom and for switching the memory circuit between a first mode and a second mode of operation". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements.

Independent claim 63 includes a memory circuit having "control logic for providing a selected mode control signal" and "a first multiplexer for receiving the first external address and the selected mode control signal ... [and] a second multiplexer ... for receiving the second external address and the selected mode control signal". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements.

Independent claim 66 includes a memory circuit having "control logic for providing a selected mode control signal" and "a multiplexer coupled to the ... control logic for receiving the ... mode control signal ... and for switching the memory circuit from a pipelined mode to a burst mode." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements.

To the elements of independent claim 66, dependent claim 67 adds "logic ... to receive an external mode select signal for selecting the burst mode". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 66, dependent claim 68 adds "mode circuitry for providing the ... mode control signal ... coupled for receiving an enable signal for determining the ... mode control signal." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To this dependent claim 68, dependent claim 69 further adds an "enable signal [that] is a write enable signal." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements. To this dependent claim 69, dependent claim 70 further adds an "enable signal [that] is an output enable signal." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 66, dependent claim 71 adds "selection and temporary storage circuitry ... coupled to a counter". Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

To the elements of independent claim 66, dependent claim 72 adds that "the pipelined mode and the burst mode are extended data out modes." Neither Manning (864) nor Manning (503), or any proper combination of the two references, disclose this combination of elements, and no other claim has this unique combination of elements.

9. SUMMARY

It is respectfully submitted that neither has a *prima facie* case of anticipation under 35 U.S.C. §102 been established, nor has a *prima facie* case of obviousness under 35 U.S.C. §103 been established. Therefore, it is respectfully requested that the rejection of claims 22-32, 59, 61, 63, and 66-72 be reconsidered and withdrawn so that the claims will be in condition for allowance. The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned attorney, to facilitate prosecution of this application. Should the Board be of the opinion that any rejected claim is allowable in amended form, an explicit statement to that effect is also respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

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P.O. Box 2938
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(612) 349-9587

Date 4 Feb 2003 By _____

Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: BOX AF, Commissioner of Patents, Washington, D.C. 20231, on this 4th day of February, 2003.

Amy Moriarty
Name

_____
Signature

APPENDIX I

The Claims on Appeal

22. A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode.

23. A memory circuit, as in Claim 22, wherein the control logic is adapted to receive an external mode select signal for selecting the burst mode or the pipelined mode and for determining the selected mode control signal.

24. A memory circuit, as in Claim 22, wherein the control logic includes mode circuitry for providing the selected mode control signal, the mode circuitry coupled for receiving an enable signal for determining the selected mode control signal.

25. A memory circuit, as in Claim 24, wherein the enable signal is selected from a group consisting of write enable and output enable signals.

26. A memory circuit, as in Claim 22, wherein the selection and temporary storage circuitry is coupled to a counter.

27. A memory circuit, as in Claim 26, wherein the counter is used for incrementing the first external address when in the burst mode.

28. A memory circuit, as in Claim 26, wherein the selection and temporary storage circuitry is coupled for receiving the first external address and a second external address subsequent thereto for operating in the pipelined mode.

29. A memory circuit, as in Claim 28, wherein the pipelined mode and the burst mode are extended data out modes.

30. A memory circuit, as in Claim 29, wherein the pipelined mode and the burst mode have no column address strobe cycle latency during a write cycle.

31. A memory circuit, as in Claim 30, wherein the pipelined mode and the burst mode have at least a two column address strobe cycle latency during a read cycle.

32. A memory circuit, as in Claim 26, wherein the memory circuit is incorporated in an asynchronously-accessible random access memory.

59. A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit between a burst mode and a pipelined mode, wherein the memory circuit is an asynchronous dynamic random access memory circuit.

61. A memory circuit, comprising:

control logic for providing an internal mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the internal mode control signal respectively therefrom and for switching the memory circuit between a first mode of operation and a second mode of operation.

63. A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first and a second external address;

a first multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom;

a second multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the second external address and the selected mode control signal respectively therefrom, wherein each multiplexer selects its respective external address when the selected mode control signal indicates a pipeline mode, and each multiplexer selects a supplied internal address when the selected mode control signal indicates a pipelined mode.

66. A memory circuit, comprising:

control logic for providing a selected mode control signal;

selection and temporary storage circuitry for receiving and storing a first external address; and

a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving the first external address and the selected mode control signal respectively therefrom and for switching the memory circuit from a pipelined mode to a burst mode.

67. The memory circuit of Claim 66, wherein the control logic is adapted to receive an external mode select signal for selecting the burst mode and for determining the selected mode control signal.

68. The memory circuit of Claim 66, wherein the control logic includes mode circuitry for providing the selected mode control signal, the mode circuitry coupled for receiving an enable signal for determining the selected mode control signal.

69. The memory circuit of Claim 68, wherein the enable signal is a write enable signal.

70. The memory circuit of Claim 68, wherein the enable signal is an output enable signal.

71. The memory circuit of Claim 66, wherein the selection and temporary storage circuitry is coupled to a counter, and wherein the counter is used for incrementing the first external address when in the burst mode.

72. The memory circuit of Claim 66, wherein the pipelined mode and the burst mode are extended data out modes.

APPENDIX II

Reference

I. Other References

"Burst Extended Data Output RAM (BEDO)", Shuttle Inc., Frequently Asked Questions, December 14, 1999

Company

Shuttle Connecting Learning

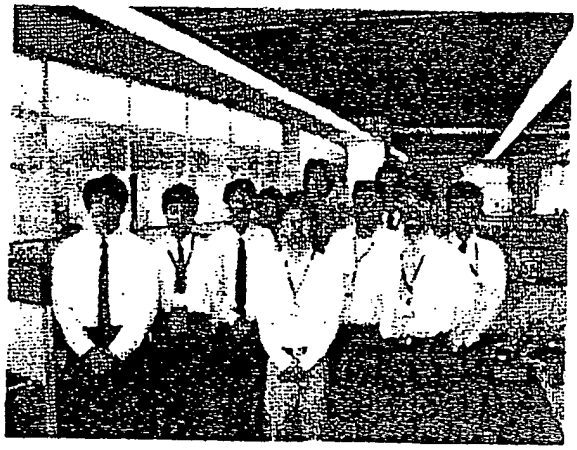
SHUTTLE - Your Ultimate Source for PC

SHUTTLE INC., headquarters of Shuttle Gro
Taiwan based manufacturer and supplie
mainboards and add-in cards. Ever since its
1983, SHUTTLE has always been recc
international markets for delivering produc
technology together with exceptional quality a
Today, SHUTTLE has become one of the
manufacturers in the world with sales rever
US$200 millions. Its Shuttle ™ and Spacewa
have already reached millions of satisfied c
wide!

Sales, Service and Support

SHUTTLE is a multi-national company with a strong commitment in customer service. Regional sales offices are located in the United States, Germany, Italy, Poland and Taiwan. Localization plus reliable after sales service and prompt technical support have enabled SHUTTLE to maintain a strong relationship with its customers including system integrators, VARs, OEMs, ODMs and distribution network.

In order to ensure round-the-clock service & support, SHUTTLE is accessible by E-mail, Web site and BBS.



Research and Development

The Research and Development engineers
highly experienced and creative. For 1!
professionals are always in pursuit of i
maintaining product's price per performance
quality. Fully equipped with hi-end CAD too
intensive research of up-to-date technology,
professionals at SHUTTLE have provided super
have been proven in the market for over a dec

Manufacturing

SHUTTLE is dedicated to TQM (Total Quality Management) principles. Only genuine brand name components are used in the products and strict QA/QC procedures are followed in the

manufacturing process. The manufacturing facilities feature the latest in SMT equipment and manufacturing technology. ISO9001, ISO9002, and ISO14000 certified, SHUTTLE's factories yield the total production capacity of over 300K units per month. In order to keeping pace with its rapidly expanding global markets, SHUTTLE is in the process of increasing its manufacturing capacity as additional SMT lines are implemented.

Environmental Policy

Our company is a member of the global
together with the whole global enterprises t
the green environment. We are dedicated
protection of the environment and the
environmental pollution, for the minimizing o
handling of energy conservation, as well as to
related legal requirements. This is to allow th
be able to have our manufactured green p
eventually protect our environment.

Our commitments:

- Strictly implement the laws and regulations
- Continuously improve the measures for preventing pollution
- Re-use the recyclable resources
- Conserve energy which shall be done by everyone
- Aspire for green products

Commitment to Customers

SHUTTLE strongly believes in teamwork partnership with customers and remains firmly committed to delivering products with the highest quality, optimum performance and value.

SHUTTLE Contact List

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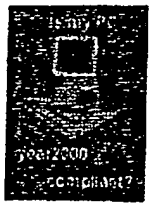
939 Radecki Court City of Industry, CA
91748, U.S.A.
TEL: 626-820-9000
FAX: 626-820-5060
http://www.shuttleonline.com


Germany Sales Office:
Shuttle Computer Handels G
Fritz-Strassmann Str. 5
D-25337 Elmshorn, Germany
TEL: 49-4121-476860
FAX: 49-4121-476900

Shuttle - Connecting Technologies



Frequently Asked Questions

SIMMs and DIMMs

Chapter set below:
SIMMs (Single In Line Memory Modules)
DIMMs (Dual In Line Memory Modules)

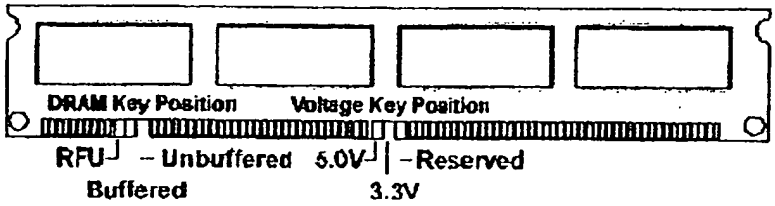
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as fas as PCs are concerned, DIMMs are at present only used for SDRAM.

SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:
Fast Page Mode (FPM)
Extended Data Output RAM (EDO)
Burst Extended Data Output RAM (BEDO)
Synchronous Dynamic RAM (SDRAM)

Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2-2.

Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e. tcas is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100"-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

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